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Development of a photonic integrated circuit (PIC) that outperforms current ubiquitous integrated circuits
Optical computing
Commercialization Plan

Elevator Pitch: Photonic integrated circuits revolutionize integrated circuits by combining both photonics and electronics. It is estimated that, if successful, photonic circuits could easily surpass current transistors speeds while also being relatively easy to produce using common fabrication techniques. All cutting edge areas that are in need for large computational power will greatly benefit from this device. This novel technology is economically and technologically feasible with the potential for a substantial revenue stream.

Executive Summary:

The purpose of this project is to design and simulate a photonic circuit that is capable of overcoming the limitations currently associated with integrated circuits, which are reaching their physical size minimums. Miniaturization of transistors is proving itself to be more and more problematic and becoming prohibitively expensive. A promising novel technology, photonic integrated circuits, has been viewed as the holy grail to this problem. By combining both photons and current technological advancements in electronics, this alleviates the miniaturization problem in electronics. In this project, a photonic 1-bit adder was designed as a proof of concept capable of solving the aforementioned problem while also being cost-effective. This approach expands upon the current advancements in photonics. A proof of concept was developed through 3D modeling a circuit that was later rigorously simulated and characterized to ensure functionality. The analysis of the simulation provided encouraging data on the performance of the circuit compared to current electronics. The technique used to simulate the circuit was based upon the fundamental theories of lightwave propagation which provides highly accurate data. The proof of concept has overcome the daunting burdens faced by the electronics industry which continually improve their technologies through miniaturization.

Problem Summary and Proposed Solution:

Microelectronics have for the past 50 years been developing according to Moore's law which states that transistor counts in chips every 19 months would be doubled (Vivien & Pavesi, 2016). Since then, Moore's law has been a driving force in the development of microelectronics. Today, the burden of innovating and improving computer chip performance is through the miniaturization of transistors (Vivien & Pavesi, 2016). Today, there are some processors that contain billions of transistors and the dimensions of these transistors are only a few tenths of a nanometer. Prohibitively increasing costs and complex extreme ultraviolet (EUV) lithography machines needed to fabricate better chips yearly is becoming ever more difficult. Currently, technologies such as photonic integrated circuits (PICs) that utilize photons to act as the medium for information have been developed and advanced over the past two decades to minimize transistor counts, increase clock speeds, and lessen signal propagation time.

In the last decades, PICs have emerged as a promising solution to the ubiquitous integrated circuits (ICs) to reduce signal propagation as well as increase bandwidth, efficiency, and clock rates. While PICs have numerous advantages, ICs contain billions of transistors, whereas current integrated photonic circuits contain only a hundred different components with the burden of high production cost (Vivien & Pavesi, 2016). The curvilinear and non-uniform design of PICs is difficult to approximate rectangularly when etching the layout onto a wafer (Chrostowski & Hochberg, 2015). This brings up the concern for the range variations within the etched waveguides. For example, corrugations within the etching resulting in a less efficient waveguide. Lastly, the processes to manufacture PICs are highly specialized as most of these systems utilize different materials to provide ultimate performance and are usually incompatible with other components. However, they are produced in specialty fabrication facilities in very low volumes (Chrostowski & Hochberg, 2015). This results in extremely high-cost components, making it difficult to produce such devices on a high-volume scale that is comparable to the current electronics industry. Thus, it is imperative to innovate to overcome the costly manufacturing of PICs, while providing superior performance, and high efficiency in a cost-effective manner.

To provide a solution to ever-aging ICs, a prototype photonic adder circuit was simulated and designed as a proof of concept. The prototype chip uses Y-branches to separate and combine beams of light. Additionally, the prototype chip has no active components (components that rely on an external power source) to increase the feasibility and decrease additional energy consumption. This prototype is far superior to conventional computer chips in clock speeds, in signal propagation time, and can import telecommunication speeds.

Summarize the STEM Concepts and Principles Underlying the Overall Plan:

To process the data entering the chip, which is light, is through the underlying concepts of constructive and destructive interference of light. Lightwaves can be thought of as an oscillation wave. **Figure 1** below illustrates constructive and destructive interference. When two beams of light intersect with each other, they produce a resultant beam of light. If the resultant beam of light has greater amplitude than the originals, this is known as constructive interference. Oppositely, if the resultant beam of light sums in no light or lower amplitude light, then this is known as destructive interference. Another STEM concept utilized in this project is the photoelectric effect. This effect describes the interaction between incident photons and electrons. For example, when a material is bombarded with electromagnetic radiation, electrons are emitted from the material known as photoelectrons. These are then later collected through an electrical current. When designing the photodetector (the component that is sensitive to light) it must use a material that is reactive to the wavelength of light in the chip in order for it to produce an electrical current. This enables a system capable of converting an optical signal to an electrical signal. The prototype uses germanium as the primary material for the photodetector since it is highly sensitive to near-infrared light.

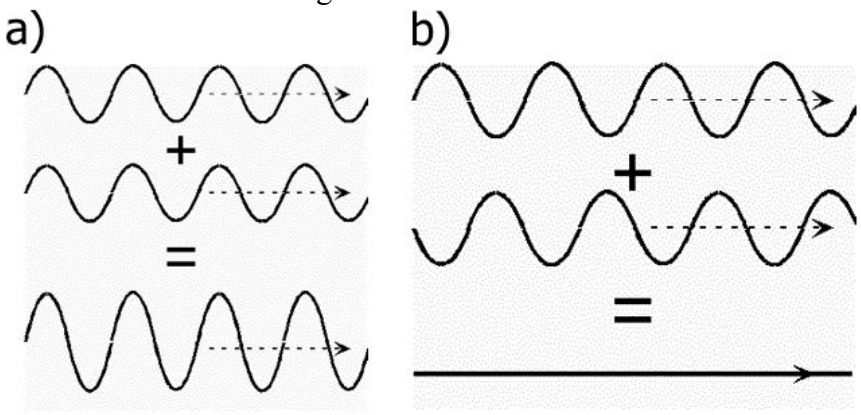

Figure 1 Image (a) represents constructive interference of light. Image (b) represents destructive interference of light.

(Gibson, 2020)

Commercialization Assessment of the Overall Plan:

Problem, pain point or market opportunity:

Key hardware problems in designing high-speed computers involve circuit density, device speed, and circuit interconnection (Hill et al., 2000). At the gate level, the main driver of energy dissipation is the capacitance of the wires repeatedly being charged and discharged, which amounts to about 200 aF/μ (attofarads per micron of wire). To lower signal propagation,

this requires more energy to charge and discharge the wires. This poses a serious sustainability issue since the consumption of energy for billions of transistors incurs large energy penalties. Additionally, transistors are reaching their ultimate size limit on semiconductors which poses another obstacle to the development of the components (Kelsall et al., 2005). Further size reductions are likely to require radically innovative approaches such as transistors based on single molecules which hinders progress to develop faster chips and promotes substantially higher fabrication costs (Kelsall et al., 2005). A promising technology to meet these aforementioned predicaments are photonic chips capable of using larger component sizes while permitting efficiency and performance. Therefore, there is an urgent need for technology that is versatile, cost-effective, contemporarily compatible, and has low distribution costs allowing it to be introduced into the market at a large scale to meet demands.

Proposed solution:

The proposed solution is to simulate a prototype photonic 1-bit adder circuit. It is important that the design of the circuit doesn't have any active components. This makes the fabrication process and fabrication time economical and feasible for mass production. Furthermore, the chip uses an onboard laser to input light from electrical input to transmit to a photonic signal which later is detected as an electrical output. The size of the components onboard the chip will remain much larger than current sizes on ICs today for ease of fabrication. Onboard the chip, there will be predominantly Y-branches to collimate and separate the beams of light. This approach removes any additional complexity in the fabrication process. Through this, the myriad of *economical benefits* and *computational advantages* will be appreciated.

Currently as far as the author knows, there is only one patent that describes the design of a photonic computer. The shortcomings of this patent is the cumbersome design of using mirrors controlled by motors and utilizes fibre optic cables (Rietman, 2002). The patent also does not claim the use of etched waveguides to act as the guide for the light, but rather the use of fibre optic cables for matrix multiplication. Additionally, the patent does not describe the novel technology of using nanometer size components to process the information imputed.

Target customers and intended users:

The largest target customers and intended users would be datacenters, gaming, and digital art studios. The gaming audience is mainly orientated towards having top-level hardware. According to Steam Hardware & Software Survey, 34.14% of individuals on Steam use a CPU that has 4 cores or above. For the past few years, the majority of new CPUs that have been released on the market by AMD and Intel have mainly been four cores or above. For digital art studios, they would benefit tremendously from improved hardware to accelerate their daily workflows. Texturing 3D models is a very computationally intensive task; especially when using average hardware. Digital artists can spend up to $3,000 per computer per year to keep up with the current standard and over time this can be very costly. Data centers contain the same internal components as any laptop or smartphone, but they are designed to withstand greater rigor and perform faster. Inside data centers are thousands of server racks that each cost tens of thousands of dollars. These datacenters, for example at NOAA (National Oceanic and Atmospheric Administration) simulate terabytes of weather data daily to provide to the general public for safety. To keep up with the ever-expanding internet and large data sets, data centers continually replace and upgrade their systems. Therefore, they would be another primary target customer and intended user.

Competitors:

Companies, including Optalysys and Lightmatter, market very limited production PICs that are specialized for deep learning algorithms. Both of these competitors blend light to process data but due to high prototyping and production costs, this renders them with many economic shortcomings, preventing high volume production. Evidently, their capabilities are only small-scale production with very specialized chips resulting in a limited application.

Customer value proposition & competitive advantage:

A computer chip or system capable of high performance while maintaining low energy consumption and high scalability is a novel technology that would be invaluable. This would be both economically and ecologically beneficial for many businesses. The PIC uses advanced optical technologies to process high volumes of data very fast and efficiently. Overall, this chip features components capable of operating at three orders of magnitude faster than today's cutting edge chips. Scalability inherent with PICs allows for many more configurations of a system. The estimated cost to fabricate a 25-mm^2 PIC using silicon as the substrate is $1350 ($350 for operating costs; $200 for fabrication; test and packaging about $800) assuming that this chip is manufactured at a high volume facility with a batch size of 100,000 units. With this novel technology, the price of this chip is clearly justified as it provides more three orders of magnitude performance for a cost that undercuts top level chips. The PIC can streamline data processing as it is able to perform in multiple roles, either as a hardware accelerator to pre-process data or act as an agonistic processing unit.

Principal revenue streams expected:

The principal revenue stream that is expected from PICs would be from licensing the chipset design to tech companies (e.g. Google, Microsoft, IBM etc.) and a 2.0% royalty rate of the profit generated from the sales. The licensing agreement would include 100,000 chips fabricated using the author's patented chip design. This upfront, licensing fee would be negotiated through lawyers and legal agreements and would expect to gross $3,375,000. The upfront fee was determined by calculating the total estimated profit that the business would make. By multiplying the total units fabricated (100,000 units) by the cost to manufacture ($1,350 per unit), and the estimated selling price of the chip (2.5×). Then, by taking 1% of this value, results in the upfront fee cost. The remaining revenue from the chipset design comes from a flat 2% share of the business' profit from sales; typical royalty rates vary from 1.0 to 3.0%.

Principal startup and operating costs expected to be incurred

Table 1 below represents the financial analysis of the business' expected profit and expenditures over a three year period. The initial startup cost is necessary to prototype two PICs. The author contacted the Design Offering Director at AIM Photonics, Mr. Bart Bergman, regarding the cost to manufacture two PIC chips at a size of 25-mm^2. The expected cost to manufacture, test, and package the two chips is $30,000. The initial prototypes will be fabricated at AIM Photonics facility in their Multi-Project Wafer (MPW) run. The author anticipates multiple design patents to be filed resulting in a projected cost of $15,000. During the patent process, DRC (Design Rule Checking) software would be utilized to ensure the chip layout/footprint meets the standards and requirements for fabrication. To simulate the chip, Lumerical™ nanophotonic software will be used. The cost of Lumerical™ is $1,500 quarterly.

Computer hardware is estimated at $6,000. To date, progress has been made in the design of the chip in the following areas: component libraries, PCells (Parameterized cells), simulations, and a germanium photodetector. It is estimated that after the initial design phase, two full-time hardware engineers (paid $90 per hour) for six months are needed to design and parameterize cells to automate the design process of the chip layout ($5,400). Office space is required for the business at a cost of $150 per person per month ($3600). Marketing (attending events, trade shows, and in-person meetings, etc.) will cost $3,000 per attendance. A domain name and website hosting will increase the viewership of the product, incurring $250 quarterly. Protection of the business' assets and electronic data from attacks, viruses, or ransomware caused by hackers through General Liability (GL) and Business Income for Electronic Vandalism (BIEV) insurance ($1,000 quarterly). Accounting services for the business helps to structure its finances and potentially help avoid penalties ($500 quarterly) would be required. Lawyer's fees to draft specially tailored agreements between the author and potential clients are estimated to cost $15,000 ($300 per hour×50 hours).

	Q1 - Designing Layout	Q2 - Prototyping	Q3 - Testing and Packaging	Q4 - Testing and Packaging	Year 2 - Marketing	Year 3 - Licensing
Incurred Costs and Expenses						
Patent Filing and examination	-$15,000.00	-	-	-	-	-
Marketing of product (Events, Tradeshows etc.)	-	-	-	-	-$15,000.00	-$15,000.00
Lawyer (licensing agreement)	-	-	-	-	-	-$15,000.00
Domain and Website	-$250.00	-$250.00	-$250.00	-$250.00	-$1,000.00	-$1,000.00
Form and maintain business	-$1,000.00	-$1,000.00	-$1,000.00	-$1,000.00	-$4,000.00	-$4,000.00
Software	-$1,500.00	-$1,500.00	-$1,500.00	-$1,500.00		
Hardware	-$6,000.00	-	-	-	-	-
Transportation	-$432.00	-$432.00	-$432.00	-$432.00	-$1,728.00	-$1,728.00
Office Space (Rented)	-$1,350.00	-$1,350.00	-$1,350.00	-$1,350.00	-$5,400.00	-$5,400.00
Consultants	-$5,400.00	-$5,400.00	-	-		
Travel (Hotel, food, etc.)	-	-	-	-	-$3,000.00	-$3,000.00
Accounting services (taxes, finances etc.)	-$500.00	-$500.00	-$500.00	-$500.00	-$2,000.00	-$2,000.00
Insurance (GL and BIEV)	-$1,000.00	-$1,000.00	-$1,000.00	-$1,000.00	-$4,000.00	-$4,000.00
Revenue						
Licensing	-	-	-	-	-	$3,375,000.00
Bank Loan	$30,000.00	-	-	-	-	-
Business Plan						
Deploying Markov decision trees	-	-	-	-	-	-
Total	-$9,932.00	-$9,932.00	-$4,532.00	-$4,532.00	-$36,128.00	$3,323,872.00

Table 1 Three year financial analysis.

Science and Technology Proof of Concept:

Review and assessment of the scientific literature:

Y-branch:

The Y-branch is a component capable of splitting the incoming light adiabatically into two outgoing waveguides, or inversely, capable of combining two beams of light. It serves as a light splitter usable for designing nanophotonic circuits. Zhang et al. (2013) demonstrated that by combining both the finite-difference-time-domain (FDTD) methods and Practice Swarm Optimization (PSO), a much more efficient Y-branch could be designed.

Grating coupler:

The basic structure that composes a grating-coupler is a periodically repeating structure with arced or linear grating teeth (Taillaert et al., 2006). This allows the structure to reflect specific wavelengths of light and is transparent to all others. AWGs (Arrayed waveguide gratings) are optical components capable of acting as optical filters and have been successfully integrated into photonic chips (Marchetti et al., 2017). An optimization experiment conducted by Marchetti and his research team (2017) resulted in a linear grating-coupler with varying etch depths that developed a high-efficiency coupler. The experimental results showed that the coupler had an efficiency above 80%. In comparison, Tailaert et al. simulated and fabricated a grating coupler to avoid unwanted second-order reflections using a gold mirror. To measure the

coupling efficiency, researchers performed transmission measurements by injecting light into the coupler and determined the value to be 69% (Taillaert et al., 2006).

Germanium Photodetector:

The purpose of the photodetector is to convert encoded optical signals into electrical signals. The structure of the photodetector consists of a substrate, absorbing medium (germanium), and a contact material that is electrically conductive. In a paper by Tseng et al., a Ge/Si photodetector was presented and fabricated to characterize the optical performance of the device (Tseng et al., 2013). The absorbing medium was created by using surface tension between the Ge and Si.

Discussion of your findings with relevant cited references:

In past research, a photonic 1-bit photonic adder circuit using 3 waveguides was successfully designed and simulated. The footprint of the 1-bit photonic adder was 0.54μm^2. Aziz-Morad et al. designed an optical full-adder based using photonic crystals which incorporates five optical waveguides (Aziz-Morad et al., 2019). It was shown that the full-adder circuit had an average delay time of less than 2ps, a data rate of more than 0.5 THz, and a footprint size of 72μm^2. According to the author's FDTD simulation of the circuit, analysis of the simulation showed that the theoretical operating frequency of the 1-bit photonic adder is 2.16 THz with a delay of 0.461 ps. In comparison to electron-based transistors, the photonic adder circuit is ~357 times faster than electron-based transistors in delay.

Statement of engineering design: A high frequency and low signal propagation photonic 1-bit adder will be designed and simulated as a proof of concept.

Inquiry or design-based discussion:

Nanophotonic wires and device geometry:

The optical guides (waveguides) serve to guide the light down the specific paths of the circuit. In order to do so, the composition of the waveguide includes a transparent material (cladding) and a high refractive index material that forms the core. **Figure 2** at the right depicts the structure of the waveguide. The principle of surrounding a high refractive index material with a transparent one allows confining the light inside the core. The light reflects at the intersection between the two materials (Rigny, 2018). The design of the circuit uses silicon (core) as the optical medium and is surrounded by SiO_2. This enables the functionality for the circuit to have bends which forms the basis for much of the components' shapes. As the light travels through the bends, the bends cause some of the light to "leak" outside the waveguide. Hence, the bend radius on the components of the circuit was kept above 50 nm to reduce much of the attenuation. Traditionally, it is standard in most integration photonic systems to have a standard dimension for the cross-section. Since the circuit operates on 1550nm light, the dimensions of the cross-section were 500nm width by 220nm height. This way, the light is more confined towards the center of the core as it travels, decreasing attenuation.

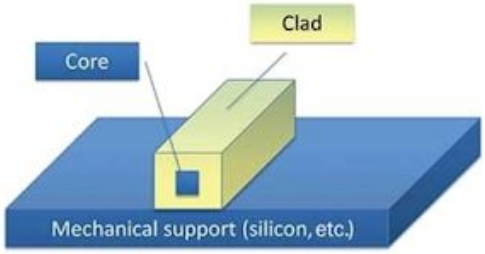

Figure 2 The image displays the general structure of waveguides.

(Rigny, 2018)

Photodetector:

The photodetector is a key device that receives and converts optical signals then outputs them as electrical signals. This is known as an O/E converter (Optical to electrical). Germanium is a material that is a good absorbing material (1310 nm light and above) and can be easily integrated into manufacturing lines for integrated photonics circuits (Piels & Bowers, 2016). The germanium has to be the contact point on the waveguide where the light interacts with it which is then connected to a conductive material. For simulation purposes, the conductive material is a pure electrical conductor with no losses. If the photodetector were to be fabricated, the material that would replace the pure electrical conductor would be gold. In this fashion, the data that is being processed gets converted from an optical signal and outputted as an electrical signal. The top layer of the photodetector is connected by a contact pin which receives the electrical signals. **Figure 3** above depicts a cross-sectional schematic of the germanium photodetector used in the circuit.

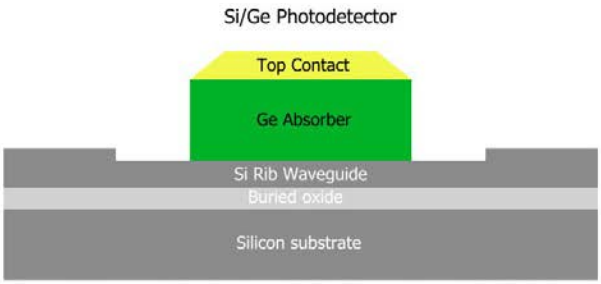

Figure 3 Cross-sectional schematic for Germanium photodetector. The illustration shows a Si/Ge photodetector. Top contact is generalized since many materials can be used. Illustration by author.

Prototyping/proof of concept:

The photonic 1-bit adder was designed in CAD using Lumerical™ nanophotonic suite. **Figure 4** illustrates the CAD model/design. The length of the circuit is 1000nm by 540nm. The circuit was made by using Y-branches from the Lumerical library with a few modifications to better suit the design study. The germanium photodetector was designed with multiple iterations to meet fabrication requirements. The germanium intersects with a waveguide taper that disperses the light and attenuates it quickly. Therefore, there is *minimal* reflection off of the detector, increasing performance.

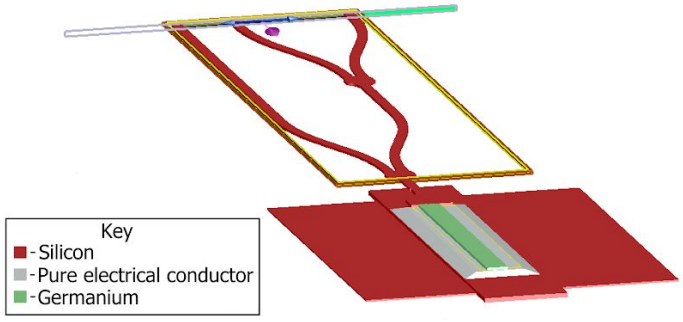

Figure 4 Orthographic view of the photonic 1-bit adder. Photo by author.

Simulation and analysis:

The approach taken to verify the optomechanics of the circuit was an FDTD simulation. The images shown in **Figure 5** below represent the simulation in chronological order. Each of the images depicts the electrical field intensity in the y-direction (E_y). In previous research, the simulation time was a continuous five day period. In **Figure 5** below, the images do not include the photodetector. It was predetermined that the inclusion of the photodetector in the simulation boundary was unnecessary because it does not affect the circuit elements involved in the calculations. Therefore, the Y-branches and waveguide taper were only included in the simulation. After setting up the simulation boundary, the CAD model of the circuit was then meshed (polygonized) so that the computer was able to average the tiny dimensions of the circuit. The meshing accuracy was set to a value of two in Lumerical™. At every junction of the Y-branches, an analysis node ($50nm^2$ in size) was set up to analyze the optical force. Another simulation region was designated to the photodetector to analyze the frequency distribution and

the highest frequency response. In this manner, the data compiled gives an overview of the performance of the circuit.

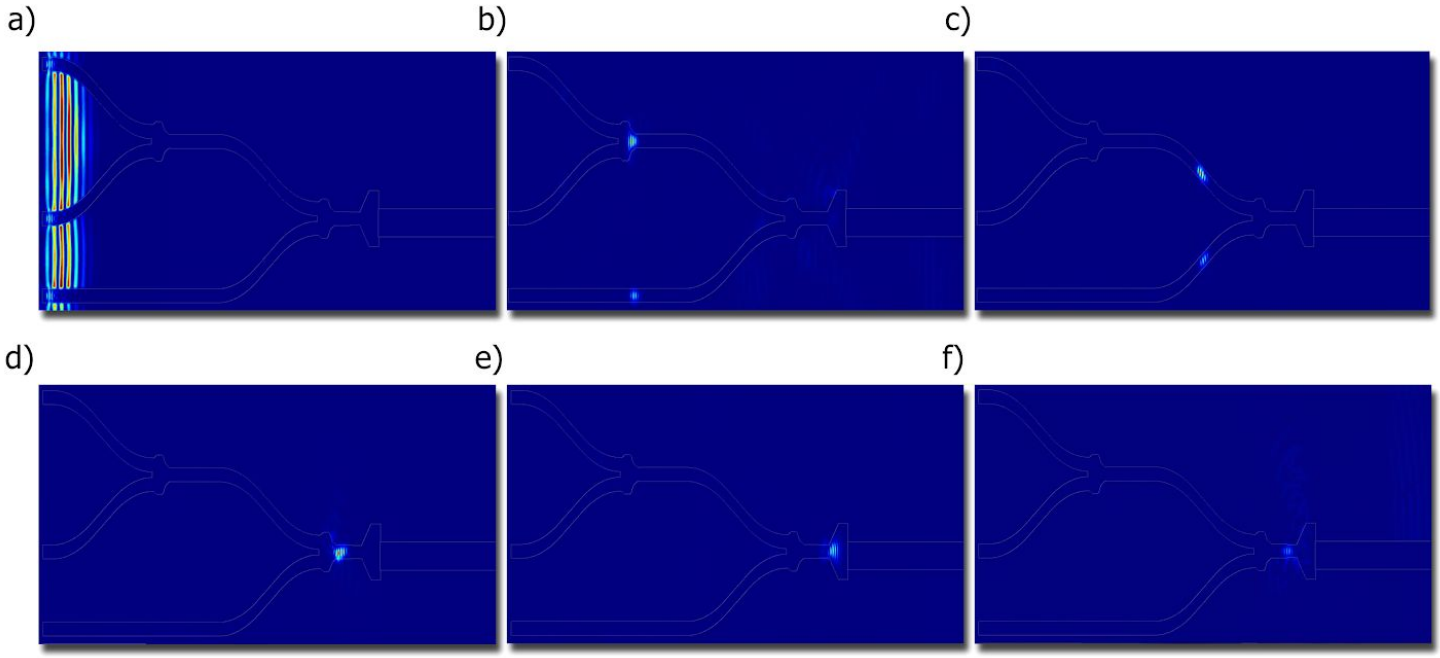

Figure 5 FDTD simulation of circuit in chronological order (alphabetically). The colors respresent the electrical field intestiy in the y-axis (E_y). Image (a) is the moment light is injected into the circuit. Image (b) illustrates the collimation of light at the Y-branch. Image (c) shows the light traveling down the waveguide. Image (d) shows the light collimating again. Image (e) shows the light being dispersed into the photodetector. Lastly, image (f) shows the light reflected off the photodetector. Photos by author.

In **Figure 5**, the colors represent the electrical field intensity in the y-direction (E_y). The data was extracted from the simulation and then processed into a video. Initially, the simulation was set up with a simulation time of 600fs (an arbitrary value that was estimated). To determine the time taken per operation, the video was imported into Blender (a 3D modeling software), capable of a frame by frame analysis. In this manner, it is possible to determine the total time taken per operation. The following equation was computed to determine the calculation time.

$$\frac{F_{final}-F_{initial}}{F_{total}} \cdot 600fs = \text{calculation time}$$

F_{final} and F_{inital} represent the final frame and first frame in the FDTD simulation respectively. F_{total} means the total number of frames within the simulation. The ratio between the difference in final and initial frames and the total frames represents the percentage of the simulation that is the circuit computing. Then it is multiplied by the total simulation time and hence, it is the theoretical total calculation time.

Data and Results:

Using the aforementioned methods in the simulation and analysis section, the theoretical total time per calculation was determined to be 461.538 fs. In contrast to the fastest electron-based transistor (604 GHz), the author's photonic 1-bit adder was capable of 2.16 THz (Hafez & Feng, 2005). This is ~3.58 times faster than Hafez and Feng's (2005) transistor. Note that the fastest electron-based transistor has not been implemented in any IC on the market and was purely for experimentation.

Figure 6 displays the optical force at each Y-branch junction in the transistor. The force-induced is perpendicular to the beams of light ("Like Magnets, Light Can Attract and Repel Itself," 2009). Therefore, beams of light can be converge or diverge. The optical forces displayed in **Figure 6** are nearly symmetrical in the middle and are indicated by the red line. When the two beams of light intersect at the Y-branch junction, there is a chance that the two beams of light may not collimate properly. In **Figure 6**, the two halves are separated by the red line. Based on the color differences between the two halves, it was determined that the probability of an improper intersection would be ~2×10^{-9} %.

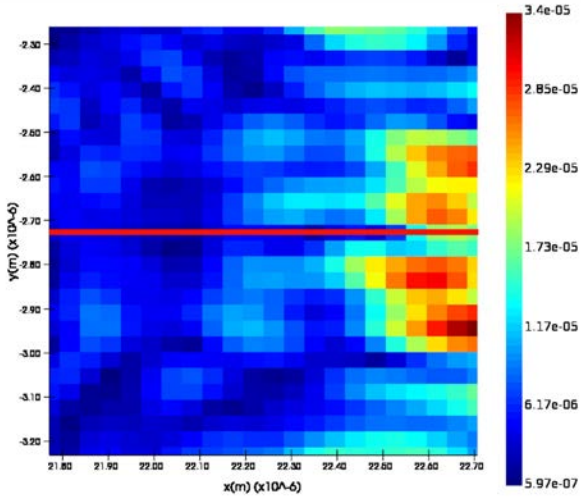

Figure 6 Optical force average at each Y-branch junction. Photo by author.

As the incident photons collide with the germanium photodetector, they are absorbed and generate electron-hole pairs which are then collected through the contact pin. The left edge of the image is where the incident photons hit the germanium in the circuit. This indicated since the color on the left edge of the image is a color that indicates a higher E_y intensity. The electrical field appears to propagate throughout the germanium evenly indicated by the brighter bands. This means that the photodetector will produce a stable electrical current as an output.

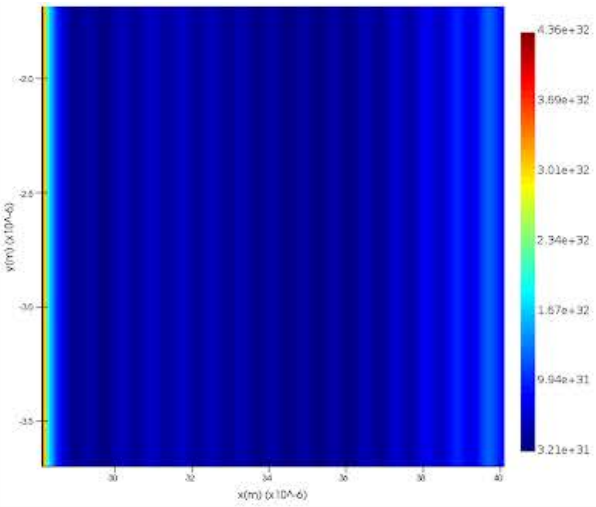

Figure 7 Electrical field intesity (E_y) propogating through the photodetector. Photo by author.

In the future, more complex prototypes, simulations, and tests will need to be done to assess the true performance of the circuit and its ability to be introduced into the market as a product. Numerical simulations will need to be made to optimize the circuit elements and layouts to improve the performance. On a large scale, complex architectures could very well undermine the performance of these transistors if not designed properly. Optical semiconductors such as InP, GaAs, and SiGe are all materials (substrates) that need to be simulated against silicon. These materials all have economical and performance benefits over each other. For example, SiGe provides high-speed performance with low power consumption and is ideal for high volume low-cost productions. On the other hand, GaAs has high electron mobility for optoelectronic components but is costly to manufacture chips on a high volume. The material's properties will be determined through real-life experimentation and implemented in an FDTD simulation. Therefore, additional research will need to be done on these materials to determine which one is ideal. The workflow for designing more complicated prototypes with large, complicated structures needs to be streamlined with PCells. With large

structures, it becomes an issue to manually design complicated circuits. PCells are components of circuits that are dependent on parameters imputed by the designer. This makes the workflow much more comprehensible when designing large structures. To determine the feasibility of the chip being introduced into the market, it has to be fabricated. This gives a glimpse as to whether the chip can be introduced into many current systems without issue or additional modifications.

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References Cited:

Vivien, L., & Pavesi, L. (2020). *Handbook of Silicon Photonics* [Google Books]. CRC Press. https://books.google.com/books?id=6zjNBQAAQBAJ&printsec=frontcover#v=onepage&q&f=false

Chrostowski, L., & Hochberg, M. (2015). *Silicon Photonics Design: From Devices to Systems*. Cambridge: Cambridge University Press. doi:10.1017/CBO9781316084168

Hill, M. D., Jouppi, N. P., & Sohi, G. S. (2000). *Readings in computer architecture* [Google Books]. Morgan Kaufmann. https://www.google.com/books/edition/Readings_in_Computer_Architecture/I7o8teBhz5wC?hl=en&gbpv=0

Kelsall, R. W., Hamley, I. W., & Geoghegan, M. (2005). *Nanoscale science and technology*. John Wiley & Sons. https://books.google.com/books?id=nVXZibKF6koC&printsec=frontcover&source=gbs_ge_summary_r&cad=0#v=onepa ge&q&f=false

Rietman, E. A. (2002). *Optical Computing* (U.S. Patent No. WO 02/25395 A2). U.S. Patent and Trademark Office. https://patents.google.com/patent/WO2002025395A2/en

Yi Zhang, Shuyu Yang, Andy Eu-Jin Lim, Guo-Qiang Lo, Christophe Galland, Tom Baehr-Jones, and Michael Hochberg, "A compact and low loss Y-junction for submicron silicon waveguide," Opt. Express 21, 1310-1316 (2013)

Marchetti, R., Lacava, C., Khokhar, A. *et al.* High-efficiency grating-couplers: demonstration of a new design strategy. *Sci Rep* 7, 16670 (2017). https://doi.org/10.1038/s41598-017-16505-z

Taillaert, D., Laere, F. Van, Ayre, M., Bogaerts, W., Thourhout, D. Van, Bienstman, P., & Baets, R. (2006). Grating Couplers for Coupling between Optical Fibers and Nanophotonic Waveguides. *Japanese Journal of Applied Physics*, 6071-6077. https://doi.org/10.1143/JJAP.45.6071

Tseng, C.-K., Chen, W.-T., Chen, K.-H., Kang, Y., Neil, N., & Lee, M.-C. (2013). A self-assembled microbonded germanium/silicon heterojunction photodiode for 25 Gb/s high-speed optical interconnects. *A self-assembled microbonded germanium/silicon heterojunction photodiode for 25 Gb/s high-speed optical interconnects.* https://doi.org/10.1038/srep03225

Vali-Nasab, A.-M., Mir, A., & Talebzadeh, R. (2019). Design and simulation of an all optical full-adder based on photonic crystals. https://doi.org/ 10.1007/s11082-019-1881-1

Rigny, A. (2018, Spring). *Silicon-on-Insulator Substrates: The Basis of Silicon Photonics*. Photonics Media. Retrieved December 30, 2020, from https://www.photonics.com/Articles/Silicon-on-Insulator_Substrates_The_Basis_of/A63021

Photodetectors for silicon photonic integrated circuits [PDF]. (2016). https://optoelectronics.ece.ucsb.edu/sites/default/files/2017-06/piels16photodetectors.pdf

Hafez, W., & Feng, M. (2005). Experimental demonstration of pseudomorphic heterojunction bipolar transistors with cutoff frequencies above 600 GHz. *Applied Physics Letters*, *86*(15), 1-3. [152101]. https://doi.org/10.1063/1.1897831

Ornes, S. (2009, December 24). *Like Magnets, Light Can Attract and Repel Itself*. Discover. Retrieved January 3, 2021, from https://www.discovermagazine.com/the-sciences/83-like-magnets-light-can-attract-and-repel-itself